COMPUTER FORMULATION OF SYMBOLIC STATE EQUATIONS FOR ANALOG NONLINEAR CIRCUITS WITH EXCESS ELEMENTS

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Abstract. A new method to systematically formulate the state equations in symbolic normal-form for nonlinear time-invariant analog circuits with excess elements is presented. For this, we have developed an algorithm, so that a computer program called **SYSEG** – **SY**mbolic **S**tate **E**quation **G**eneration was written to formulate the symbolic normal-form equations of a large class of nonlinear analog circuits. These circuits may contain both linear and nonlinear resistors, inductors, and capacitors, independent voltage and current sources, and the four types of linear controlled sources. Our program allows the formulation of symbolic state equations without any inverse of a symbolic matrix, and, by cancellation and simplification of the expressions, it obtains a symbolic compact form. Degeneracies of the first kind are unitary treated in order to allow a symbolic representation of the circuit with a minimum number of state variables. Illustrative examples are given to prove that our program is a very useful tool for symbolic analysis and design of nonlinear time-invariant analog circuits.

Index Terms – nonlinear circuits, excess elements, state equations, eigenvalues, poles and zeros.

I. INTRODUCTION

The classical design of analog integrated circuits is based on a mixture of expertise, some calculations, and numerical circuit simulation. The results obtained in the last years in the field of symbolic circuit analysis begin to have a considerable impact on the traditional design flow.

In this paper we propose a simple and efficient method to automatically formulate the state equations in a symbolic normal-form, for large time-invariant nonlinear analog circuits. Starting from the circuit description in the netlist form, our method is based on Kirchhoff's laws, constitutive equations of the circuit elements, and it uses the facilities of symbolic simulator Maple V.

Because numerical differentiation is a relatively inaccurate operation, we approximate the $q_k - v_k$ curve of each nonlinear capacitor and the $\varphi_k - i_k$ curve of each nonlinear inductor by piecewise-linear segments. In order to simplify the description of nonlinear resistors, their $v - i$ curves may be approximated by piecewise-linear continuous curves, or by new curves in which the nonlinearities are transferred to the sources.

Using the state equations in symbolic form, we obtain an important efficiency in circuit design, and an improving of the accuracy in the numerical calculations. Also, by a straightforward analysis, the coefficients of the characteristic polynomial can be computed exactly, in order to detect the eigenvalues at the origin. In this way it easy to estimate an optimal discretisation time step in relation with eigenvalues of the state-matrix, (which are the roots of the characteristic polynomial). So, the smallest eigenvalue (largest time constant) allows estimating a total simulation time, and the largest eigenvalue (smallest time constant) facilitates the choice of the size of a time step.

In Section II the standing assumptions on the class of allowable circuits are exposed. In Section III we present the procedure of symbolic formulation for state equations. In Section IV the SYSEG program is described, and meaningful examples are found in Section V.

II. STANDING ASSUMPTIONS ON THE CLASS OF ALLOWABLE CIRCUITS

To avoid certain types of circuits, whose symbolic normal-form equations either do not exist or are pathological, in the sense that their order of complexity depends on *the precise* value of some element parameters, we assume that the analyzed circuits meet the following requirements:

1. *Consistency assumptions*
   a) There are not any loop consisting only of independent and/or controlled voltage sources, henceforth called an *E loop*;
   b) There are not any cutset made up only of independent and/or controlled current sources, henceforth called an *J cutset*;
   c) All nonlinear capacitors are voltage-controlled. This means that the charge q of each capacitor is a function of its voltage, $q = \hat{q}(v)$;

d) All nonlinear inductors are current-controlled. This means that the flux linkage φ of each inductor is a function of its current, $\varphi = \hat{\varphi}(i)$;

2. *Normal tree assumptions*

a) A special tree called *normal tree* (*NT*) is chosen. The normal tree has to contain in this priority: all independent and controlled voltage sources, all nonlinear voltage-controlled resistors, as many capacitors as possible, as many controlling branches of the current-controlled voltage sources and of the current-controlled current sources as possible (these branches are considered as resistive branches having the resistances equal to zero), and as many resistors as possible. It will not contain any independent and controlled current source, and any nonlinear current-controlled resistor;

b) Any controlled source belonging to a *C-E* loop or an *L-J* cutset can depend only on the voltage of a tree capacitor or on the current of a link inductor.

Though most practical circuits do not violate these assumptions, regarding the last one, we can note that there are many circuits which although don't meet it, they have state equations in normal-form yet, [15].

III. FORMULATION OF SYMBOLIC STATE EQUATIONS

Let *N* be a nonlinear network containing both linear and nonlinear resistors, inductors, and capacitors, independent voltage and current sources, linear magnetic couplings, the four types of linear controlled sources, and any multiterminal circuit elements having an equivalent scheme made up only of two-terminal circuit elements and controlled sources. The inductors and current derivative-controlled voltage sources, [9,15], can simulate the magnetic couplings.

According to the above assumptions a normal tree is selected, and the essential incidence matrix is corresponding partitioned. The capacitors that are not included in the normal tree are called *excess capacitors*, and the inductors that are included in the normal tree are called *excess inductors*.

The curve *i-v* (*v-i*) of each voltage-controlled (current-controlled) nonlinear resistor is approximated by piecewise-linear continuous curve, and corresponding to segment *s*, it has the following form:

$$i_{vk} = G_{vdk}(s)v_{vk} + j_{vk}(s) \tag{1, a}$$

$$e_{vk}^{-}(s) \le v_{vk} \le e_{vk}^{+}(s), \tag{1, b}$$

for a voltage-controlled (v.c.) nonlinear resistor, and

$$v_{ik} = R_{idk}(s)i_{ik} + e_{ik}(s) \tag{2, a}$$

$$j_{ik}^{-}(s) \le i_{ik} \le j_{ik}^{+}(s), \tag{2, b}$$

for a current-controlled (c.c.) nonlinear resistor.

Also, the nonlinear element characteristic $y = \hat{y}(x)$ of any nonlinear resistor can be replaced by

$$y = \alpha x - \hat{s}(x) \tag{3}$$

where

$$\hat{s}(x) = \alpha x - \hat{y}(x), \tag{4}$$

and the parameter α is a resistance (a conductance) if the quantity *y* is a voltage (a current), [12,13].

In [12] it is shown that if for any nonlinear circuit element we choose an optimal value for the parameter α, thus:

$$\alpha = \frac{\alpha_{\max} + \alpha_{\min}}{2}, \tag{5}$$

in which $\alpha_{\max}, \alpha_{\min}$ are the maximum, respectively, minimum values of the slopes of the nonlinear characteristic $y = \hat{y}(x)$, then the iterative process is convergent for any starting value of *x*, provided that $y = \hat{y}(x)$ is a Lipschitzian and uniform continuous increasing characteristic. In this case, the characteristic $\hat{i}(u)$ of a voltage-controlled nonlinear resistor has the expression:

$$\hat{i}(u) = G_0 u - \hat{j}(u) \tag{6, a}$$

with

$$\hat{j}(u) = G_0 u - \hat{i}(u) \tag{6, b}$$

and

$$G_0 = \frac{G_{d,\max} + G_{d,\min}}{2}, \tag{6, c}$$

where $G_{d,\max}$ and $G_{d,\min}$ are the maximum, respectively, minimum values of the differential conductances of the voltage-controlled nonlinear characteristic $\hat{i}(u)$.

The characteristic $\hat{u}(i)$ of a current-controlled nonlinear resistor has the expression:

$$\hat{u}(i) = R_0 i - \hat{e}(i) \tag{7, a}$$

with

$$\hat{e}(i) = R_0 i - \hat{u}(i) \tag{7, b}$$

and

$$R_0 = \frac{R_{d,\max} + R_{d,\min}}{2}, \tag{7, c}$$

where $R_{d,\max}$ and $R_{d,\min}$ are the maximum, respectively, minimum values of the differential resistances of the current-controlled nonlinear characteristic $\hat{u}(i)$.

We assume that the voltage vector of the controlled voltage sources $\boldsymbol{v}_{E_c}$ and the current vector of the controlled current sources $\boldsymbol{i}_{J_c}$ can be expressed in respect to the resistor voltages or resistor currents or state variables. Since there are at least two possible state variables that might be chosen for each capacitor (its voltage or charge) and for each inductor (its current or flux linkage), there are many possible combinations of state variables for a given circuit. A suitable choice for the state variables is the tree capacitor voltage vector $\boldsymbol{v}_{Ct}$ and the link inductor current vector $\boldsymbol{i}_{Ll}$.

According to Kirchhoff's laws, and to the constitutive equations of circuit elements, we obtain the following symbolic form of state equations:

$$\left[\boldsymbol{C}_{dt}(\boldsymbol{v}_{Ct}) + \boldsymbol{D}_{CC} \cdot \boldsymbol{C}_{dl}(\boldsymbol{v}_{Cl}) \cdot \boldsymbol{D}_{CC}^{\mathrm{t}}\right]\frac{\mathrm{d}\boldsymbol{v}_{Ct}}{\mathrm{d}t} = -\boldsymbol{D}_{CL}\boldsymbol{i}_{Ll} - \boldsymbol{D}_{CR}\boldsymbol{i}_{Rl} - \boldsymbol{D}_{CJ_c}\boldsymbol{i}_{J_c} - \boldsymbol{D}_{CJ_i}\boldsymbol{i}_{J_i} -$$
$$- \boldsymbol{D}_{CC} \cdot \boldsymbol{C}_{dl}(\boldsymbol{v}_{Cl}) \cdot \boldsymbol{D}_{E_cC}^{\mathrm{t}}\frac{\mathrm{d}\boldsymbol{v}_{E_c}}{\mathrm{d}t} - \boldsymbol{D}_{CC} \cdot \boldsymbol{C}_{dl}(\boldsymbol{v}_{Cl}) \cdot \boldsymbol{D}_{E_iC}^{\mathrm{t}}\frac{\mathrm{d}\boldsymbol{v}_{E_i}}{\mathrm{d}t} \tag{8, a}$$

$$\boldsymbol{v}_{Cl} = \boldsymbol{D}_{E_iC}^{\mathrm{t}}\boldsymbol{v}_{E_i} + \boldsymbol{D}_{E_cC}^{\mathrm{t}}\boldsymbol{v}_{E_c} + \boldsymbol{D}_{CC}^{\mathrm{t}}\boldsymbol{v}_{Ct}, \tag{8, b}$$

and, respectively

$$\left[\boldsymbol{L}_{dl}(\boldsymbol{i}_{Ll}) + \boldsymbol{D}_{LL}^{\mathrm{t}} \cdot \boldsymbol{L}_{dt}(\boldsymbol{i}_{Lt}) \cdot \boldsymbol{D}_{LL}\right]\frac{\mathrm{d}\boldsymbol{i}_{Ll}}{\mathrm{d}t} = \boldsymbol{D}_{CL}^{\mathrm{t}}\boldsymbol{v}_{Ct} + \boldsymbol{D}_{RL}^{\mathrm{t}}\boldsymbol{v}_{Rt} + \boldsymbol{D}_{E_cL}^{\mathrm{t}}\boldsymbol{v}_{E_c} + \boldsymbol{D}_{E_iL}^{\mathrm{t}}\boldsymbol{v}_{E_i} +$$
$$- \boldsymbol{D}_{LL}^{\mathrm{t}} \cdot \boldsymbol{L}_{dt}(\boldsymbol{i}_{Lt}) \cdot \boldsymbol{D}_{LJ_c}\frac{\mathrm{d}\boldsymbol{i}_{J_c}}{\mathrm{d}t} - \boldsymbol{D}_{LL}^{\mathrm{t}} \cdot \boldsymbol{L}_{dt}(\boldsymbol{i}_{Lt}) \cdot \boldsymbol{D}_{LJ_i}\frac{\mathrm{d}\boldsymbol{i}_{J_i}}{\mathrm{d}t} \tag{9, a}$$

$$\boldsymbol{i}_{Lt} = -\boldsymbol{D}_{LL}\boldsymbol{i}_{Ll} - \boldsymbol{D}_{LJ_c}\boldsymbol{i}_{J_c} - \boldsymbol{D}_{LJ_i}\boldsymbol{i}_{J_i}. \tag{9, b}$$

The signification of the matrices and vectors from Eqs. (8) and (9) is given by their subscripts. For example $\boldsymbol{D}_{CL}$ $(\boldsymbol{D}_{RL})$ represents the incidence submatrix of the link inductors to the cutsets associated to the tree branch capacitors (resistors), and $\boldsymbol{v}_{Cl}$ $(\boldsymbol{i}_{J_i})$ is the link capacitor voltage vector (the current vector of the independent current sources).

From Eqs. (8) and (9) we have to eliminate the variables $\boldsymbol{v}_{Rt}, \boldsymbol{i}_{Rl}, \boldsymbol{v}_{E_c}$, and $\boldsymbol{i}_{J_c}$. If the controlling variables of the controlled sources belong to the state vector or if they are variables associated to the resistors, these equations represent a set of nonlinear equations in respect to the independent variables $\boldsymbol{v}_{Rt}$ and $\boldsymbol{i}_{Rl}$. Assuming that for any specified $\boldsymbol{v}_{Ct}, \boldsymbol{i}_{Ll}, \boldsymbol{v}_{E_i}$, and $\boldsymbol{i}_{J_i}$ these nonlinear equations have a unique solution, they can be solved

by an iterative procedure (for example Newton-Raphson algorithm) at each time instant t_j. Using the symbolic simulator Maple V, [16], we obtain, for the time instant t_j, the symbolic expressions of the variables $\boldsymbol{v}_{Rt}, \boldsymbol{i}_{Rl}, \boldsymbol{v}_{E_c}$, and $\boldsymbol{i}_{J_c}$, corresponding to the arbitrary segment combination *s*. In order to eliminate the variables $\boldsymbol{v}_{Rt}$ and $\boldsymbol{i}_{Rl}$ we can use both the piecewise-linear approximation for nonlinear resistors (Eqs. (1), (2)) and the nonlinear source method (Eqs. (2)-(7)), obtaining the following equations:

$$\boldsymbol{G}_{vdt}(s)\cdot\boldsymbol{v}_{Rt} + \boldsymbol{D}_{RR}\boldsymbol{i}_{Rl} + \boldsymbol{D}_{RJ_c}\boldsymbol{i}_{J_c} = -\boldsymbol{D}_{RL}\boldsymbol{i}_{Ll} - \boldsymbol{D}_{RJ_i}\boldsymbol{i}_{J_i} - \boldsymbol{j}_{vt}(s) \tag{10, a}$$

$$-\boldsymbol{D}_{RR}^{\mathrm{t}}\boldsymbol{v}_{Rt} + \boldsymbol{R}_{idl}(s)\cdot\boldsymbol{i}_{Rl} - \boldsymbol{D}_{E_cR}^{\mathrm{t}}\boldsymbol{v}_{E_c} = \boldsymbol{D}_{CR}^{\mathrm{t}}\boldsymbol{v}_{Ct} + \boldsymbol{D}_{E_iR}^{\mathrm{t}}\boldsymbol{v}_{E_i} - \boldsymbol{e}_{il}(s), \tag{10, b}$$

and, respectively

$$\boldsymbol{G}_{0t}\boldsymbol{v}_{Rt} + \boldsymbol{D}_{RR}\boldsymbol{i}_{Rl} + \boldsymbol{D}_{RJ_c}\boldsymbol{i}_{J_c} = -\boldsymbol{D}_{RL}\boldsymbol{i}_{Ll} - \boldsymbol{D}_{RJ_i}\boldsymbol{i}_{J_i} + \hat{\boldsymbol{j}}_{Rt}(\boldsymbol{v}_{Rt}) \tag{11, a}$$

$$-\boldsymbol{D}_{RR}^{\mathrm{t}}\boldsymbol{v}_{Rt} + \boldsymbol{R}_{0l}\boldsymbol{i}_{Rl} - \boldsymbol{D}_{E_cR}^{\mathrm{t}}\boldsymbol{v}_{E_c} = \boldsymbol{D}_{CR}^{\mathrm{t}}\boldsymbol{v}_{Ct} + \boldsymbol{D}_{E_iR}^{\mathrm{t}}\boldsymbol{v}_{E_i} + \hat{\boldsymbol{e}}_{Rl}(\boldsymbol{i}_{Rl}). \tag{11, b}$$

Solving Eqs. (8)-(11), we obtain the symbolic state equation in normal form

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{y} + \boldsymbol{B}_1\dot{\boldsymbol{y}}, \tag{12}$$

where matrices $\boldsymbol{A}$, $\boldsymbol{B}$ and $\boldsymbol{B}_1$ have the elements in symbolic form (see example).

IV. DESCRIPTION OF SYSEG PROGRAM

We have implemented the above algorithm on the program **SYSEG** – **SY**mbolic **S**tate **E**quation **G**eneration – which generates, starting from the circuit netlist, the state equations, for the nonlinear time-invariant analog circuits, in symbolic form. SYSEG is written in C++ language and it is implemented on the compatible IBM Pentium PC. It is a new software environment that allows the schematic representation, the analysis and design of linear or nonlinear analog circuits, even when they have excess elements. This is an interactive tool that combines symbolic and numeric computational techniques, and which uses the facilities of symbolic simulator Maple V to manipulate the symbolic expressions.

The input data of SYSEG program are:

1. *nnod*, *nb* , where *nnod* – is the number of circuit nodes, *nb* – represents the number of circuit branches.
2. It follows a set of *nb* input rows describing the circuit branches. A circuit branch is made up only of one two-terminal element or one controlled (controlling) branch for the controlled sources. The initial node, the final node, and the type of circuit element describe each circuit branch. In the case of a controlled source we have to give also the number of the controlling branch (see example).

SYSEG program has the following capabilities:

- Procedures for drawing the circuit scheme;
- Automated generation of the normal tree, identifying the excess elements;
- Automated formulation of state equations in symbolic normal form, directly from the circuit netlist;
- Symbolic evaluation of state matrix;
- Symbolic computation of characteristic polynomial, eigenvalues, and eigenvectors;
- Symbolic computation of circuit functions, poles, and zeros;
- Sensitivity analysis;
- Plotting the frequency characteristics.

V. EXAMPLE

The circuit in Fig. 1 contains an excess element (an *L*-J_i cut-set), so that the complexity order of the circuit is $b_C + b_L - n_{\Sigma_{L-J_i}} = 1+2-1=2.$). The controlling variables of the controlled sources are associated resistor variables.

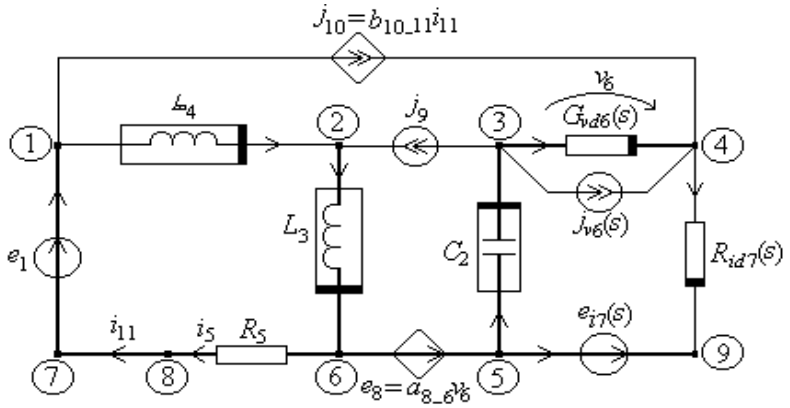

Fig. 1. Circuit with an excess element.

According to the assumptions presented above, the program generates the normal tree introducing the inductor L_3 in the tree branch set: NT={e_1, e_8, e_{i7}, C_2, b_{11}, R_5, G_{vd6}, L_3}. The state variables of the circuit are the voltage of the tree capacitor, and the current of the link inductor, {v_2, i_4}.

The symbolic state equations obtained by the program have the form:

$$od1 := \frac{\partial}{\partial t}\,\mathrm{v2}(t) = -\frac{\mathrm{Gvd6}(s)\,\mathrm{v2}(t)}{(\mathrm{Rid7}(s)\,\mathrm{Gvd6}(s)+1)\,\mathrm{Cd2}(v2)} + \frac{\mathrm{Rid7}(s)\,B10\_11\,\mathrm{Gvd6}(s)\,\mathrm{i4}(t)}{\mathrm{Cd2}(v2)\,(-1+B10\_11)\,(\mathrm{Rid7}(s)\,\mathrm{Gvd6}(s)+1)} + \frac{\mathrm{j9}(t)}{\mathrm{Cd2}(v2)} - \frac{\mathrm{Gvd6}(s)\,\mathrm{ei7}(s)}{(\mathrm{Rid7}(s)\,\mathrm{Gvd6}(s)+1)\,\mathrm{Cd2}(v2)} + \frac{\mathrm{jv6}(s)}{(\mathrm{Rid7}(s)\,\mathrm{Gvd6}(s)+1)\,\mathrm{Cd2}(v2)}$$

$$od2 := \frac{\partial}{\partial t}\,\mathrm{i4}(t) = \frac{r5\,\mathrm{i4}(t)}{(\mathrm{Ld4}(i4)+\mathrm{Ld3}(i3))\,(-1+B10\_11)} + \frac{\mathrm{e1}(t)}{\mathrm{Ld4}(i4)+\mathrm{Ld3}(i3)} - \frac{\mathrm{Ld3}(i3)\left(\frac{\partial}{\partial t}\mathrm{j9}(t)\right)}{\mathrm{Ld4}(i4)+\mathrm{Ld3}(i3)}$$

with $i_3(t) = i_4(t) + j_9(t)$.

If resistor R_5 is substituted by a linear inductor L_5, then the circuit in Fig. 1 has in addition a *L-E* loop (a degeneracy of the second kind), and the characteristic polynomial

$$polychar := \left(s + \frac{\mathrm{Gvd6}(s)}{\mathrm{Cd2}(v2)\,(\mathrm{Rid7}(s)\,\mathrm{Gvd6}(s)+1)}\right)s$$

has an eigenvalue equal to zero.

VI. CONCLUSIONS

We propose a simple and efficient method to formulate the state equations in a symbolic normal-form for large nonlinear time-invariant analog circuits. We have developed an efficient and simple algorithm so that a computer program was written to formulate the symbolic normal-form equations of a large class of nonlinear time-invariant analog circuits. These circuits may contain both linear and nonlinear resistors, inductors, and capacitors, independent voltage and current sources, and the four types of linear controlled sources. According to our method to formulate the state equations in the symbolic normal-form a program, called **SYSEG** – **SY**mbolic

State **E**quation **G**eneration, was implemented. Starting of the circuit netlist, SYSEG checks all assumptions regarding consistency and existence of normal tree, checks also if the circuit to be analyzed can be described by a set of state equations in normal form, and it specifies the type of degeneracies. If the circuit meets the standing assumptions, SYSEG automatically generates the normal tree, and finally, the state equations in symbolic normal-form. In addition, the program SYSEG has others important capabilities, offering us the state-matrix of the circuit, and the characteristic polynomial in the symbolic form, performing the time-domain analysis of the circuit for different numerical values of the circuit parameters, computing the eigenvalues and eigenvectors too.

Our method of symbolic computation to find the state equations in normal-form, without any inverse of literal matrix, greatly facilitate cancellation and simplification of expressions. Using the state equation in symbolic normal-form, an important improving of the accuracy in the numerical calculations is obtained. In the case of the linear analog circuits the state matrix in symbolic form can be used to obtain a simplified expression of any circuit function, preserving a "cluster" of poles and zeros.

By a straightforward analysis the coefficients of the characteristic polynomial can be computed exactly in order to detect the eigenvalues at the origin. In this way it is easy to estimate an optimal discretised time step in relation with eigenvalues of the state-matrix, which are the roots of the characteristic polynomial. So, the smallest eigenvalue (largest time constant) allows to estimate a total simulation time and the largest eigenvalue (smallest time constant) facilitates the choice of the size of a time step. SYSEG program is an interactive tool that combines symbolic and numeric computational techniques, and it is very easy to use. It has been tested on many and various linear and/or nonlinear analog circuits.

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